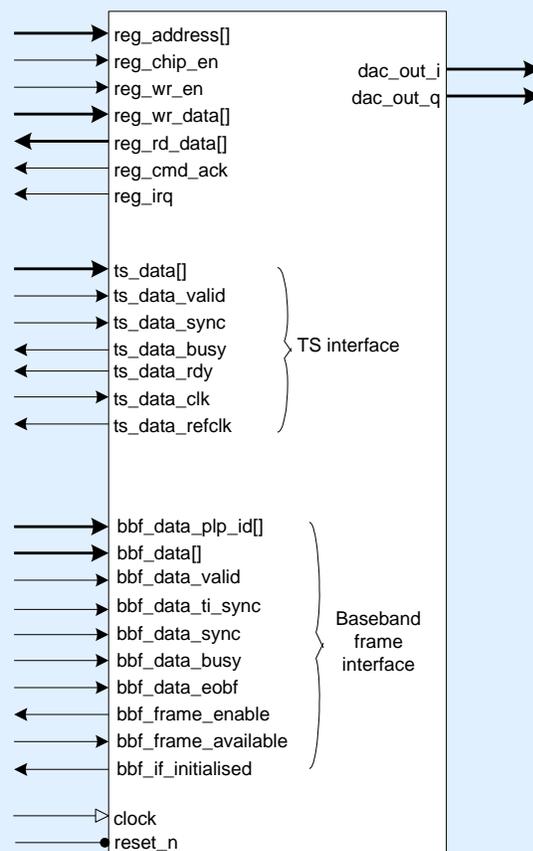- Compliant with ETSI EN 302 755 including T2-Lite.
- Enables rapid development of audio/visual systems using commodity Free-to-Air set-top-box technology and low-cost FPGAs.
- Configurable support for 1K, 2K, 4K, 8K, 16K and 32K OFDM modes.
- Integrated LDPC channel coder with short (16kb) or normal (64kb) frame support.
- Automatic L1-PRE/L1-POST padding and puncturing
- Configurable support for 1/4, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 1/3 and 2/5 code-rates.
- BPSK, QPSK, 16-QAM, 64-QAM and 256-QAM support.
- All pilot patterns supported : PP1…PP8
- SISO and/or MISO operation.
- Future Extension Frames (FEF) support.
- Optional L1-ACE and P2 bias cells processing.
- Optional CPU-free configuration.
- Optional Cell-ID, Network-ID and T2-System-ID local insertion.
- Variable channel bandwidth support using a single clock reference; 1·7MHz… 10MHz.
- AD9857/AD9957/AD9789 interface and auto-programming support.
- AD9516/ADF4350 PLL programming support.
- Extension core available for TS Adaptation featuring normal-mode or HEM operation with SPI/ASI interface and integrated PCR TS re-stamping.
- Extension core available for T2MI interface support.
- Extension core available for multiple-PLP support.
- Extension core available for SFN support.
- Extension core available for PAPR-TR support.
- Seamless integration with Altera ASI megacore when using SPI/ASI extension core.
- Optional FFT output windowing and/or in-band pre-distortion.
- Optional dual-clock architecture for increased flexibility.
- Designed for very efficient FPGA implementation without compromise to the targeting of gate array or standard cell structures.
- Supplied as a protected bitstream or netlist (Megacore® for Altera® FPGA targets).
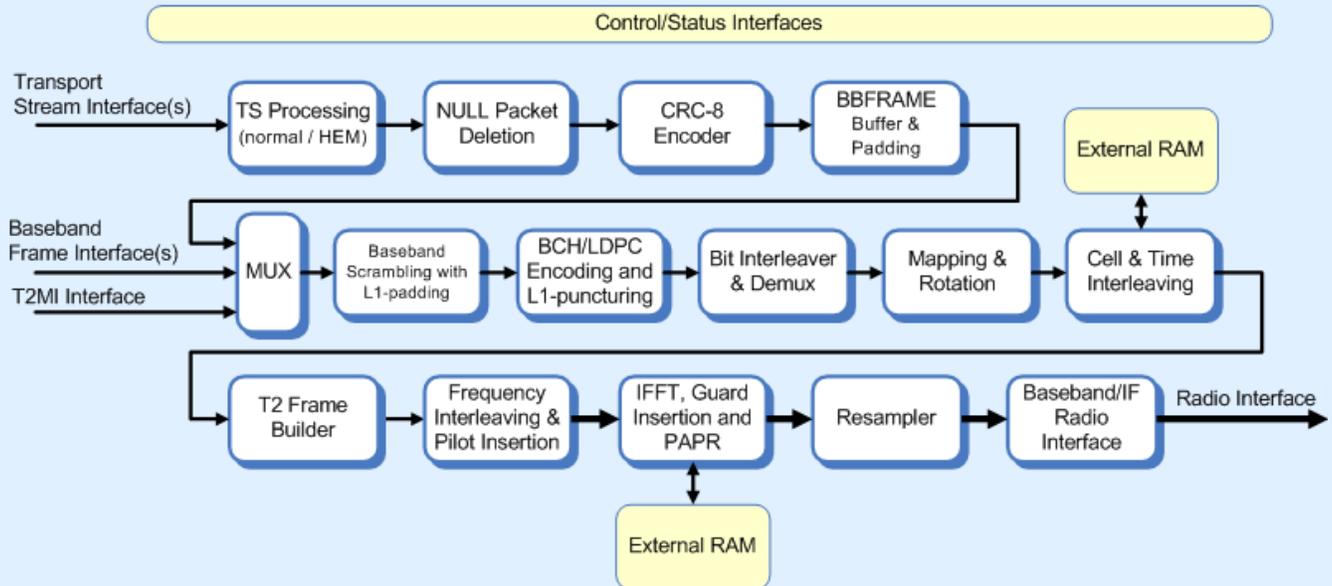
**reg_address[]**
**reg_chip_en**
**reg_wr_en**
**reg_wr_data[]**
**reg_rd_data[]**
**reg_cmd_ack**
**reg_irq**

**dac_out_i**
**dac_out_q**

**ts_data[]**
**ts_data_valid**
**ts_data_sync**
**ts_data_busy**
**ts_data_rdy**
**ts_data_clk**
**ts_data_refclk**
} TS interface

**bbf_data_plp_id[]**
**bbf_data[]**
**bbf_data_valid**
**bbf_data_ti_sync**
**bbf_data_sync**
**bbf_data_busy**
**bbf_data_eobf**
**bbf_frame_enable**
**bbf_frame_available**
**bbf_if_initialised**
} Baseband frame interface

**clock**
**reset_n**

## Contact information

## Block Diagram



## Detailed Description

The Commsonic CMS0041 DVB-T2 Modulator provides all the necessary processing steps to modulate single transport stream into a complex I/Q signal for input to a pair of DACs, or interpolating DAC devices such as the AD9857/AD9957 or RF-DACs such as the AD9789. Optionally the output can be selected as an IF to supply a single DAC.

Additional extension cores are available for multiple-PLP (common/data) support, T2MI interface support and SFN deployment support.

The design has been optimised to provide excellent performance in low cost FPGA devices such as the Cyclone™ range from Altera or the Spartan™ range from Xilinx

A description of the processing steps follows:

**TS Processing**. The TS processing block performs rate adaptation functions in Broadcast applications to ensure that variable transmission delays do not result in disturbances of time-critical services such as audio and video. Both normal-mode and High-Efficiency-Mode(HEM) processing is supported.

**Null packet deletion.** The Null packet deletion block removes null TS packets from the input stream to maximise the capacity available for information services in VCM and ACM modes. The mechanism defined by DVB-T2 allows for complete restoration of the input stream where null packets are necessary to maintain a constant delay.

**CRC-8 Encoding.** An 8-bit CRC is added to each outgoing TS packet and serves to allow packet-level error detection at the receiver.

**Baseband buffer and Padding.** The baseband padding block inserts a fixed-length Baseband Header at the start of each BBFRAME and pads to the end of the frame during ACM operation. The structure of the Baseband Header is as described in EN 302 755.

**Baseband Scrambling.** The baseband scrambler block performs the energy dispersal and transport multiplex adaptation using the DVB randomisation polynomial $1+x^{14}+x^{15}$.

When processing L1-field frames (L1PRE/L1POST), zero padding is added to ensure the non-standard L1 frame length is compliant prior to FEC encoding.

# Detailed Description (cont'd)

**BCH, LDPC Encoders.** These blocks systematically encode each frame and append error correction information bits. When processing L1-field frames (L1PRE/L1POST), puncturing is performed where necessary following FEC encoding.

**Bit Interleaver and Demux.** The bit interleaver block applies block-based and column-twist bit interleaving to the coded frame prior to symbol de-multiplexing and mapping.

**Mapping and Rotation.** This block performs the QAM constellation mapping using the mapping schemes specified by DVB for BPSK, QPSK, QAM16, QAM64 and QAM256. Optionally constellation rotation is applied as indicated by the L1FIELD information fields, together with L1-ACE modifications when enabled.

**Cell and Timing Interleaving.** This block performs both the cell and timing interleaving as dictated by the DVB-T2 specification. Typically, external memory, such as SDRAM, would be utilised for the substantial Timing interleaver storage required by the standard.

**T2 Frame builder.** The DVB-T2 specification details a frame and super-frame structure with scattered, continuous, tone-reservation and closing-symbol information inserted at various carriers within each OFDM symbol. This block manages the collation of data carriers from the various L1 & L2 encoded FECFRAMES based on the L1FIELD information fields. This block is also responsible for sequencing the appropriate OFDM symbol type information through to the subsequent pilot/guard insertion and IFFT processing stages.

**Frequency interleaving and Pilot insertion.** The DVB-T2 standard specifies a number of OFDM size dependent frequency interleaving modes together with various pilot patterns as indicated by the embedded L1FIELD information fields. This block is responsible for both the OFDM symbol frequency interleaving and also the subsequent insertion of the pilot carriers. Both SISO and MISO configurations are supported.

**IFFT.** This block performs the Inverse Fast Fourier Transform (IFFT) on the 1k, 2k, 4k, 8k, 16k or 32k carriers as indicated by the L1PRE field. A proprietary architecture is used which yields low Guassian noise, high MER outputs yet utilises low datapath widths. The IFFT also manages the on-air timing of the OFDM symbols by guard interval insertion (1/128, 19/256, 19/128, 1/32, 1/16, 1/8 or 1/4).

An optional windowing function is also included to reduce spurious emissions caused by the OFDM symbol transitions. A further optional in-band pre-distortion can also be optionally performed.

Additionally, the DVB-T2 standard specifies a number of schemes to aid peak-to-average power reduction (PAPR) of the modulated signal. The Commsonic DVB-T2 core provides a number of techniques to utilise the hooks make available by the standard.

**Resampler.** This block re-samples the complex samples output from the IFFT into complex samples at the core clock frequency. This provides an ultra-flexible clocking strategy. This block also scales automatically as required to satisfy the selected channel bandwidth (1·7MHz, 5MHz, 6MHz, 7MHz, 8MHz or 10MHz).

**Baseband-to-IF.** This block provides the option to mix the signal up to a higher IF as defined by a software register. This block may be removed using synthesis options if it is not required.

**DAC Aperture Correction.** This optional step provides compensation for the sin(x)/x (or SINC) distortion that is introduced in the DAC. This block may be removed using synthesis options is the feature is not required.

**Radio Interface.** This block performs some final, register-selectable processing functions to optimise the output for the radio in the target application. For example, the data can be formatted to work with either twos-complement or offset-binary DAC devices. In addition the data is formatted to suit the external vice that could take separate I/Q, multiplexed I/Q or a single IF output.

Additional modes are added to support the Analog Devices AD9857(or AD9957) device that provide up-conversion, SINC filtering and DAC functions in a single package. The AD9857 device requires that the I/Q data be multiplexed onto a single data bus. The *ad9857_pdclk* input is provided to enable this feature and should be sourced from the AD9857 PDCLK output.

## Detailed Description (cont'd)

**Register Bank.** The register bank provides a simple 32-bit interface for reading and writing registers within the modulator block. Additionally the 32-bit interface is used to access the two external memories (TITL and IFFT) where necessary. Full details of the available registers and control configuration for the modulator core are contained within the full IP guide for the core.

## Principle I/O Description

| Register Bus Interface | |
|---|---|
| reg_address (I) [] | Register address select input. |
| reg_chip_en (I) | Active-high block select input for the CMS0041 register bank. |
| reg_wr_en (I) | Active-high write Enable Input for CMS0041 access. |
| reg_wr_data (I) [31:0] | 32-bit Write data input. |
| reg_rd_data (O) [31:0] | 32-bit Read data output. |
| reg_cmd_ack (O) | Active-high command acknowledge. |
| reg_irq (O) | Active-high interrupt line. |

| Transport Stream Interface | |
|---|---|
| ts_data (I) [] | 8-bit Transport Stream data. |
| ts_data_valid (I) | Transport Stream data valid. |
| ts_data_sync (I) | Transport Stream data sync. |
| ts_data_rdy (O) | Transport Stream path is ready for new byte. Data transferred when Ready and Valid are asserted together. (RDY/VLD interface). |
| ts_data_clk (I) | Transport Stream clock. (TS PCR plug-in). |
| ts_data_refclk (O) | Transport Stream reference clock. (TS PCR plug-in). |
| ts_data_busy (O) | Transport Stream interface busy.  TS data should be stalled until the interface is available again. <br> (Only relevant to ACM operation when using the TS PCR plug-in). |

| Baseband Frame Interface | |
|---|---|
| bbf_data (I) [] | 8-bit baseband frame data. |
| bbf_data_plp_id (I) [] | 8-bit baseband frame PLP IDentifier. |
| bbf_data_valid (I) | Baseband frame data valid. |
| bbf_data_sync (I) | Active-high flag indicating the first data of the frame. |
| bbf_data_ti_sync (I) | Active-high flag indicating the first data of the timing interleaver-frame. |
| bbf_data_busy (O) | Active-high flag indicating that core is busy and cannot accept any more data. |
| bbf_data_eobf (I) | Active-high flag indicating that this is the final byte of the frame. |
| bbf_frame_enable (O) | Active-high flag indicate that this interface has gained access to the modulation chain, and the frame should be input. |
| bbf_frame_available (I) | Active-high flag indicating that there is a frame ready to be input. |
| bbf_if_initialised (O) | Active-high flag indicating that the baseband-frame interface has initialised and is ready to accept data. |

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| Modulator Output Interface | |
|---|---|
| dac_out_i | 14-bit Transmit I complex output or IF output in IF mode. |
| dac_out_q | 14-bit Transmit Q complex output. |
| ad9857_txdata | 14-bit multiplexed data to the AD9857 if used. |
| ad9857_txenable | Controls the interface timing to the AD9857 if used. |
| **Others** | |
| clock | Clock input, greater than 100MHz for 10MHz bandwidth operation. |
| ad9857_pdclk | AD9857 Clock. |
| reset_n | Asynchronous active-low reset input. |

# Transport Stream Interface

## Standard TS interface:

The standard TS interface supplied uses a ready/valid handshake mechanism to allow data to be pulled through the modulator processing chain based on the on-air symbol rate.  This requires the TS data source to be stalled when the modulator core is busy.



**Data Transfer**

**TS Interface stalled due to the inactive RDY signal**
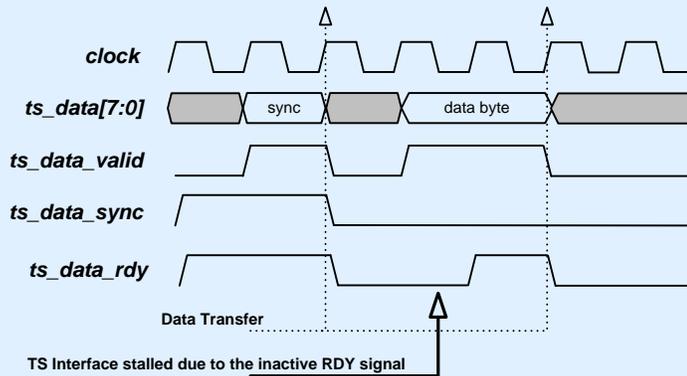
## PCR re-stamping TS interface:

Typically for broadcast applications, the input stream from the transport multiplexer is provided at a fixed rate that requires 'padding' to match the required on-air bitrate.  For this application, the Null-Packet-Deletion block cannot be used, and consequently some form of traditional MPEG TS rate adaption is required.  The TS PCR restamping extension core provides a simpler TS interface (compatible with SPI or ASI) to allow data to be input at any rate.

The core will be pad the input TS stream with NULL TS packets as required and perform any PCR adjustment.

When the PCR restamping extension core is used, an output signal, *ts_data_refclk* is provided that indicates the necessary 188-byte TS byterate to satisfy the on-air requirements for broadcast operation.

For ACM applications the core generates an additional output signal, *ts_data_busy*.  The input TS stream should be stalled whilst *ts_data_busy* is high. This allows data to be burst into the core at a higher bitrate.  Following the assertion of *ts_data_busy*, the core can accept 3 more input bytes before the cores input buffers are overflowed.



**Data Transfer**

**Interface should stop inputting valid data in response to the core asserting *ts_data_busy* (Only applicable to ACM applications)**
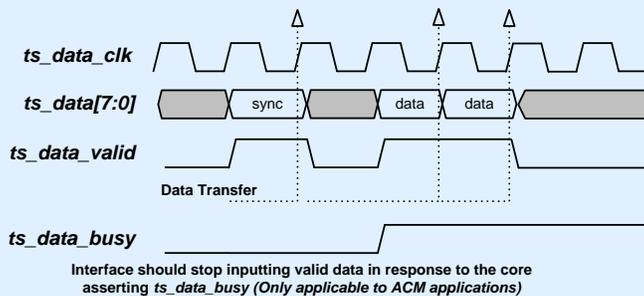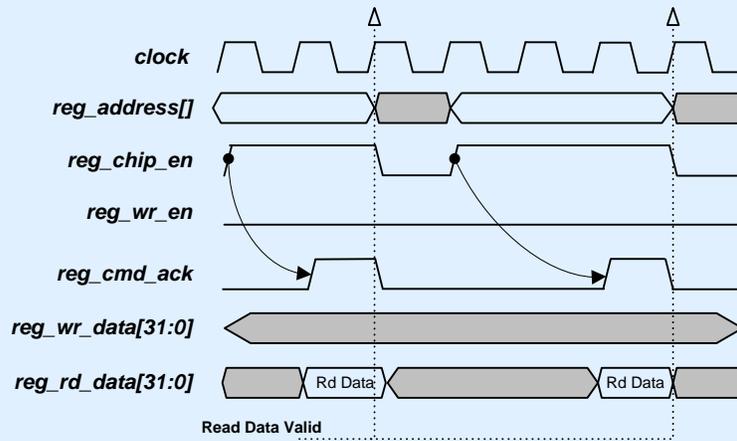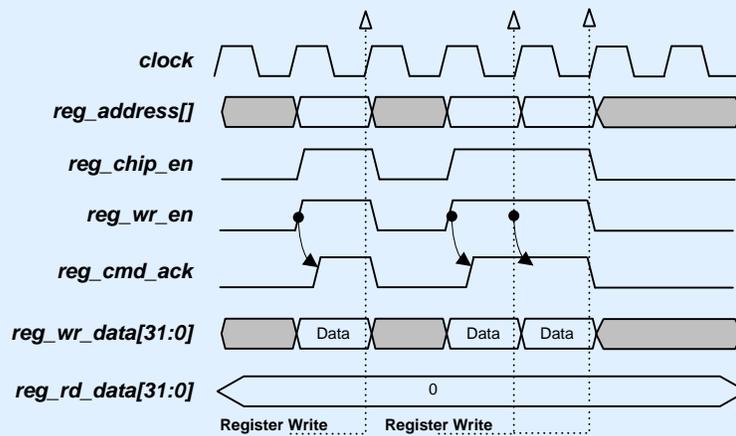
# Register Interface

A 32-bit register-programming interface is provided. The register core is intended to be interfaced to whatever host interface is appropriate for the application.

An active-high interrupt line is also available.
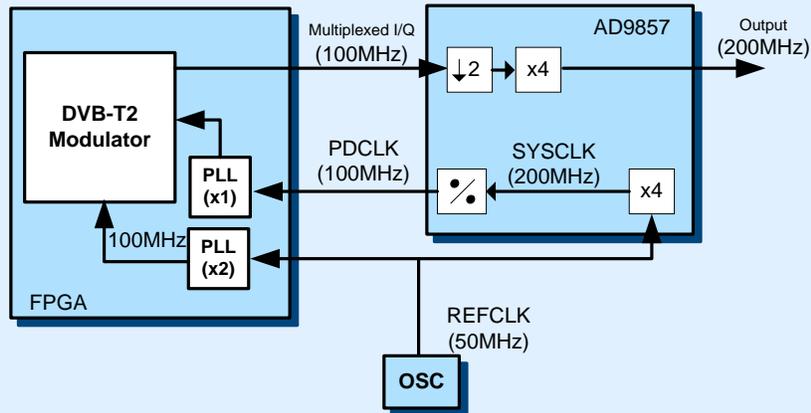
## Register read access:



## Register write access:

# Example Applications

## Up-sampled IFFT output using external up-conversion:

This application uses the DVB-T2 modulator core with internal interpolation that allows the channel bandwidth to be changed via a simple s/w register change.



## Up-sampled IFFT output using internal interpolation & up-conversion:

This application uses the DVB-T2 modulator core with internal interpolation that allows the channel bandwidth to be changed via a simple s/w register change. The DVB-T2 modulator internal up-conversion is also used which allows direct connection to external DAC devices
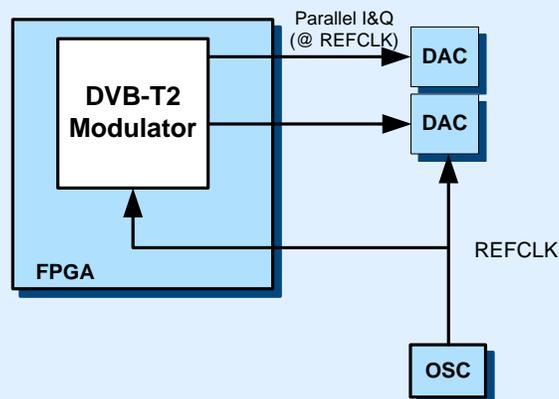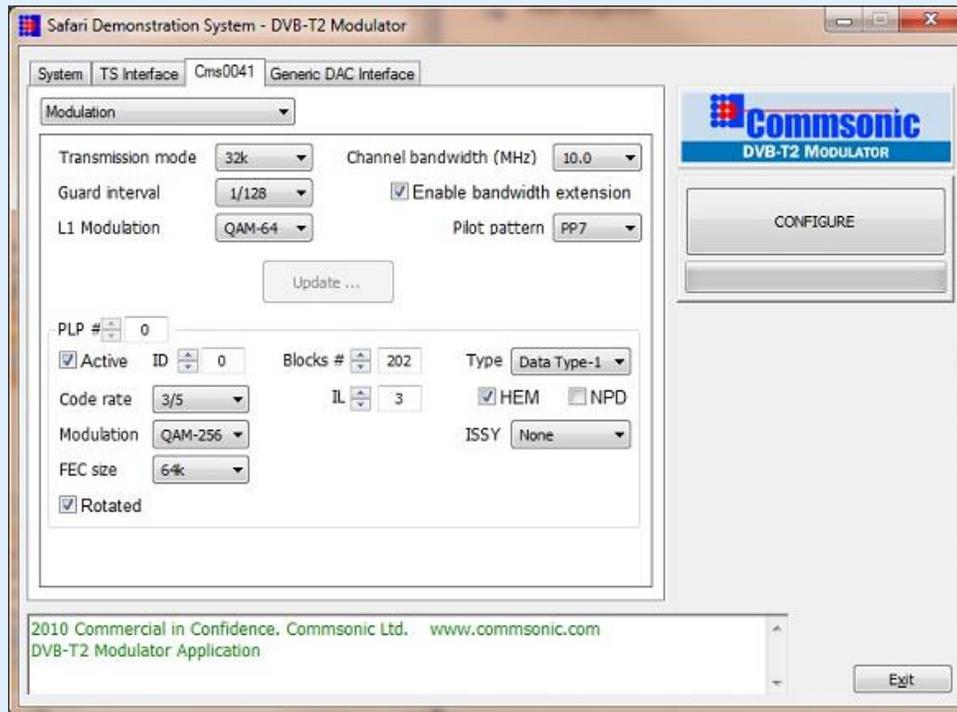
# In-band pre-distortion

The core can be optionally configured to include an in-band pre-distortion module to compensate for group-delay distortion through the analog and RF amplifier stages.
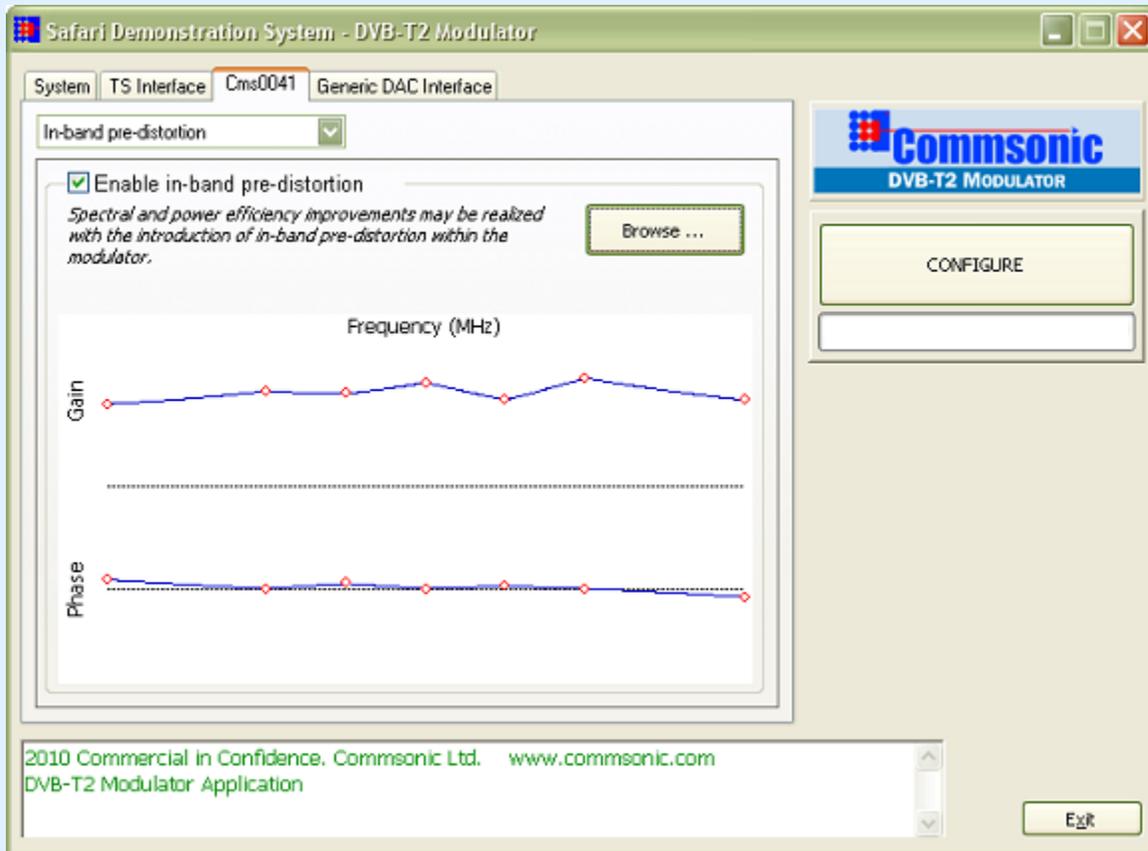
## Evaluation



## About Commsonic:

Commsonic is an IP and design services company that specialises in the development of ASIC, FPGA, DSP and board-level sub-systems for applications in wireless and wireline communications.

Our expertise is primarily in the gate- and power-efficient implementation of physical-layer (PHY) functions such as modulation, demodulation and channel coding, but we have extensive experience with all of the major elements of a modern baseband 'core' including medium access control (MAC), voiceband DSP, mixed-signal interfaces and embedded CPU and software.

Our services are available on a turn-key basis but they are usually provided as part of a support package attached to members of our expanding family of licensable IP cores.

Commsonic's IP spans the major Standards for cable, satellite and terrestrial digital TV transmission and includes high-performance, adaptable, single-carrier (QAM) and multi-carrier (COFDM) modulator and demodulator solutions for DVB-S/DSNG/S2, DVB-CID, ATSC-8VSB, DVB-C/J.83/A/B/C, DVB-T/H, DVB-T2 and ISDB-T.

Commsonic's customers are typically semiconductor vendors and manufacturers of broadband transceiver equipment that demand leading-edge Standards-based or proprietary PHY solutions but don't have the internal resources necessary to get their products to market soon enough.